

## **REMARKS**

### **Status Of Application**

Claims 1-11 are pending in the application; the status of the claims is as follows:

Claims 1-3, 8, and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable U.S. Patent Publication No. 2002/0057351 to Suzuki et al. ("Suzuki et al.") in view of U.S. Patent No. 6,380,975 to Suzuki ("Suzuki '975").

Claims 4-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2001/0001563 to Tomaszewski ("Tomaszewski"), in view of PCT International Published Application No. WO 99/40723 to Clemens ("Clemens"), in view of Suzuki et al., and further in view of U.S. Patent No. 6,567,122 to Anderson et al. ("Anderson").

Claims 9 and 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Suzuki et al., in view of Suzuki '975, and further in view of U.S. Patent No. 6,278,492 to Nakamura ("Nakamura").

### **35 U.S.C. § 103(a) Rejections**

The rejection of claims 1-3, 8, and 11 under 35 U.S.C. § 103(a), as being unpatentable over Suzuki et al. in view of Suzuki '975, is respectfully traversed based on the following.

With regard to claim 1, it is apparent, that the point being made in the prior response was not made clearly enough. Specifically, the Office Action states that "the feature '*a reconfigurable processing element may be used for anything other than a CPU*' is not recited in claim 1." The point being made was that Suzuki et al. only teaches that CPU 34 may be implemented using an FPGA or other programmable logic device. Indeed, Suzuki et al states that any circuit may be used that can implement a state machine

corresponding to the flow chart of Fig. 3 (sic – the only flow chart is shown in Fig. 6). See [0054]. Thus, the only teaching provided by Suzuki et al. is to use an FPGA to implement a CPU that implements the flow chart. Suzuki et al. does not provide any other teaching with regard to using a FPGA. We apologize for any confusion.

Moreover, it is respectfully submitted that claim 1 does in fact require a reconfigurable processing element that is not a CPU. Claim 1 recites a camera comprising, *inter alia*:

... an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data ...;

Thus, the camera of claim 1 requires a circuit that can be configured to form different logic circuits, *wherein each logic circuit performs a predetermined operation on input image data*. One skilled in the art would understand that a CPU is a general purpose device for executing software instructions. A CPU does not perform a predetermined operation on input image data, rather, a CPU executes programs. That is, the predetermined operation executed by a CPU is to read and execute software instructions. It may be the case that software being executed by a FPGA/CPU causes it to perform operations on input image data. However, that is different than configuring the FPGA to form circuits that operate on the image data directly as required by claim 1.

It is respectfully submitted that Suzuki '975 does not add anything to Suzuki et al with regard to using reconfigurable circuitry to implement image processing logic circuits. Accordingly, claim 1 distinguishes over both references as well as the combination thereof.

Claim 1 further recites a camera including, *inter alia*,

a memory for memorizing a first program corresponding to the first image data processing and a second program corresponding to the second image data processing; and

a controller for reading the first program from the memory and writing it in the electronic circuit arrangement when the first mode is selected by the mode selector and for reading the second program from the memory and writing it in the electronic circuit arrangement when the second mode is selected by the mode selector.

That is, the camera includes a controller that (re)configures the electronic circuit following a program that is selected based on an operating mode of the camera. It is admitted at page 7 of the Office Action that this is not taught by Suzuki et al. Suzuki '975 is cited as providing the missing teaching. Suzuki '975 teaches that CPU 133 executes different programs stored in MEM 114 based on an operating mode of the camera. For example, the CPU executes different programs from the memory when taking a picture (column 11, lines 53-62), printing a picture (column 12, lines 65-67), estimating time to process an image (column 13, lines 57-59), estimating the memory required to store an image (column 13, lines 66-67), and providing instructions to a user (column 14, lines 14-20), as well as many other tasks. Indeed, at page 8 the Office Action cites Suzuki '975 as teaching that CPU 113 performs image compression or decompression based on a control program stored in CPU 113.

All words in a claim must be considered in judging the patentability of that claim against the prior art. MPEP 2143.03. Claim 1 requires that the programs configure the electronic circuit arrangement to form a logic circuit that executes a predetermined operation on inputted image data. The programs taught by Suzuki '975 are merely software routines being executed by a CPU. Moreover, assuming *arguendo* that the programs taught by Suzuki '975 were configuration programs, it is respectfully submitted that Suzuki '975 does not disclose a controller that copies the programs from a memory to a reconfigurable circuit as required by claim 1. The Office Action cites the Suzuki FPGA/CPU as corresponding to the configurable electronic circuit arrangement of claim 1. One skilled in the art would understand that a CPU fetches instructions from a memory and then executes the fetched instructions. Thus, the combination of Suzuki '975 and

Suzuki et al. suggests that the FPGA/CPU *itself* fetches and executes different program instructions from memory 114 depending on the operating mode of the camera. However, claim 1 clearly recites the electronic circuit arrangement and the controller as distinct elements, and requires that the controller read the configuration programs from the memory and write them to the configurable circuit arrangement.

In light of the forgoing discussion, it is respectfully submitted that claim 1 clearly distinguishes over Suzuki '975 and Suzuki et al. regardless of whether the references are taken alone or in combination. Accordingly, claim 1 is allowable over Suzuki '975 and Suzuki et al., as are claims 2 and 3 which depend from claim 1.

Claim 8 recites, *inter alia*:

an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on image data input thereto;

a memory for memorizing a plurality of programs corresponding to the plurality of image processing; and

a controller for reading a program corresponding to the image processing selected by the image processing selector and writing it in the electronic circuit arrangement.

As set forth above in respect of claim 1, these features of claim 8 are not disclosed, taught, or otherwise suggested by Suzuki '975 and Suzuki et al. It is respectfully submitted therefore that claim 8 also distinguishes the cited combination of references, as does claim 11 which depends from claim 8.

Accordingly, it is respectfully requested that the rejection of claims 1-3, 8, and 11 under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al. in view of Suzuki '975, be reconsidered and withdrawn.

The rejection of claims 4-7 under 35 U.S.C. § 103(a), as being unpatentable over Tomaszewski, in view of Clemens, in view of Suzuki et al., and further in view of Anderson, is respectfully traversed based on the following.

Claim 4 recites a camera comprising, *inter alia*:

a connection portion to which a first equipment and a second equipment can alternatively be connected ... by a first data communication standard, and ... a second data communication standard;

a detector for judging a kind of data communication standard of an equipment connected to the connection portion;

...; and

a controller for reading the first program from the memory and writing it in the electronic circuit arrangement when the kind of the data communication standard of the equipment connected to the communication portion is judged as the first data communication standard by the detector and for reading the second program from the memory and writing it in the electronic circuit arrangement when the kind of the data communication standard of the equipment is judged as the second data communication standard.

Ascertaining the differences between the prior art and the claims at issue requires interpreting the claim language, and considering both the invention and the prior art references as a whole. MPEP 2141.02 emphasis added. Taken as a whole, claim 4 clearly requires a camera that (1) is capable of being connected to other devices according to two different communication standards, (2) detects and distinguishes which of the two different communication standards is being used, and (3) loads a selected configuration program into a configurable circuit based on the communication standards being used.

Tomaszewski teaches a digital camera that is operable in a tethered mode or in a portable mode, which mode is determined by detecting whether a voltage is present on the VBUS of a USB cable. If the voltage is present, the Tomaszewski camera assumes that the camera is connected to a USB cable and operates in tethered mode; otherwise, the camera assumes it is not connected and operates in portable mode. See Fig. 2 and paragraphs [0021] and [0022]. Thus, Tomaszewski merely teaches a camera that

determines if it is connected to a computer, but does not detect how it is connected, e.g., by USB and RS-232. Indeed, it is admitted at pages 10-11 of the Office Action, that Tomaszewski fails to disclose the second equipment being communicative with the camera by a second data communication standard. Considering that Tomaszewski does not even mention a second communication standard, it is nonsensical to hold that it teaches to distinguish between two different communication standards. It is respectfully submitted that all of the other references, i.e., Clemens, Suzuki et al, and Anderson, also fail to teach this feature of claim 4.

Claim 4 also requires "...an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on inputted image data...." As provided above in regards to claim 1, this feature of claim 4 is not taught or suggested by Suzuki et al. It is further submitted that it is not taught or suggested by any other reference of record in the present case.

In light of the foregoing is respectfully submitted that the references of record, taken singly or in combination, do not disclose, teach, or otherwise suggest the elements of claim 4, or claims 5-7 which depend therefrom.

Accordingly, it is respectfully requested that the rejection of claims 4-7 under 35 U.S.C. § 103(a) as being unpatentable over Tomaszewski in view of Clemens in view of Suzuki et al., be reconsidered and withdrawn.

The rejection of claims 9-10 under 35 U.S.C. § 103(a), as being unpatentable over Suzuki et al., in view of Suzuki '975, and further in view of Nakamura, is respectfully traversed based on the following.

Claims 9 and 10 depend from claim 8 which recites, *inter alia*:

an electronic circuit arrangement in which a logic circuit is obtained when a predetermined program is written, said logic circuit is configured depending on the written program, and said logic circuit executes a predetermined operation on image data input thereto;

a memory for memorizing a plurality of programs corresponding to the plurality of image processing; and

a controller for reading a program corresponding to the image processing selected by the image processing selector and writing it in the electronic circuit arrangement.

Claim 9 and 10 incorporate these elements of claim 8 by virtue of depending therefrom. As set forth above in respect of claim 1, these features of claim 8 are not disclosed, taught, or otherwise suggested by Suzuki V and Suzuki et al. It is respectfully submitted that Nakamura fails to cure the deficiencies of Suzuki '975 and Suzuki et al. Therefore, the subject claims also distinguishes the combination of Suzuki '975, Suzuki et al., and Nakamura.

Accordingly, it is respectfully requested that the rejection of claims 9-10 under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al. in view of Suzuki '975 further in view of Nakamura, be reconsidered and withdrawn.

### **CONCLUSION**

Wherefore, in view of the remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited.

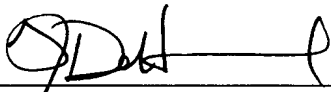
This Amendment does not increase the number of independent claims, does not increase the total number of claims, and does not present any multiple dependency claims. Accordingly, no fee based on the number or type of claims is currently due. However, if a fee, other than the issue fee, is due, please charge this fee to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260.

Application No. 09/821,442  
Amendment dated November 16, 2005  
Reply to Office Action of May 18, 2005

If an extension of time is required to enable this document to be timely filed and there is no separate Petition for Extension of Time filed herewith, this document is to be construed as also constituting a Petition for Extension of Time Under 37 C.F.R. § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

Any other fee required for such Petition for Extension of Time and any other fee required by this document pursuant to 37 C.F.R. §§ 1.16 and 1.17, other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

Respectfully submitted,

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